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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/619,884	07/15/2003	Michael Maldei	INTECH 3.0-083	7447

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EXAMINER	
KEBEDE, BROOK	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 03/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/619,884	MALDEI ET AL.	
	Examiner	Art Unit	
	Brook Kebede	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *1-27 and 38-47* is/are pending in the application.

4a) Of the above claim(s) *16-27* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15 and 38-47* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicants' submission filed on February 25, 2005 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 38-43 and 47 rejected under 35 U.S.C. 102(e) as being anticipated by Hamamoto (US/6,521,938).

Re claim 38, Hamamoto discloses a method of forming a semiconductor device, the method comprising: foaming a plurality of structures over a semiconductor body (see Fig. 31) ; forming an insulating material (41) (see Figs. 30 and 31) between ones of the structures; applying a line mask over the semiconductor body (62), the line mask exposing at least one of the structures (see Fig. 31) and regions of the insulating material adjacent opposing edges of the at least one of the structures; removing the insulating material, that is exposed by the line mask to create at least recesses, the at least two recesses being separated by as interposed structure that

was exposed the line mask, each of the recesses exposing a conductive region adjacent the interposed structure; forming a conductive material within the at least two recesses (see Fig. 32) and overlying the interposed structure, the conductive material electrically (6) (see Fig. 32) connecting the conductive regions exposed by the recesses; anal forming a layer of material over the conductive material, such that the conductive material electrically connects the conductive regions at a point in tune when the layer of material is formed (see Figs. 4-33).

Re claim 39, as applied to claim 38 above, Hamamoto discloses all the claimed limitations including the limitation wherein forming a plurality of structures comprises forming a plurality of gate stacks over the semiconductor body and wherein the conductive regions comprise doped silicon regions (23) (see Figs. 4-33).

Re 40, as applied to claim 39 above, Hamamoto discloses all the claimed limitations including the limitation wherein each gate stack forms a gate of an access transistor of a dynamic random access memory (DRAM) cell, the DRAM cell further comprising a storage capacitor coupled to the access transistor (see Figs. 4-33).

Re claim 41, as applied to claim 40 above, Hamamoto discloses all the claimed limitations including the limitation wherein the conductive material comprises a bitline contact, the bitline contact being electrically insulated from the gate stacks (see Figs. 4-33).

Re claim 42, as applied to claim 39 above, Hamamoto discloses all the claimed limitations including the limitation wherein each gate stack includes a conductor and a sidewall insulator adjacent a sidewall of the conductor, each gate stack further comprises insulating layer overlying the conductor, and wherein removing the insulating material comprises etching the

insulating material selectively with respect to the sidewall insulator and the insulating layer (see Figs. 4-33).

Re claim 43, as applied to claim 38 above, Hamamoto discloses all the claimed limitations including the limitation wherein the insulating material comprises an oxide, wherein the insulating layer and the sidewall insulator comprise a nitride, and wherein removing the insulating material comprises performing a reactive ion etch (see Figs. 4-33).

Re claim 47, as applied to claim 38 above, Hamamoto discloses all the claimed limitations including the limitation wherein forming a conductive layer comprises forming a doped polysilicon layer (see Figs. 4-33).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 1-5, 8, 44 and 45 rejected under 35 U.S.C. 103(a) as being unpatentable over Hamamoto (US/6,521,938) in view of Sung et al. (US/5,814,862)

Re claim 1, Hamamoto discloses a method of fabricating a semiconductor device, comprising; patterning a mask on a surface of a semiconductor wafer (see Figs. 18 and 19) to expose portions of the semiconductor wafer (i.e., substrate) while covering other portions of the semiconductor wafer; forming a plurality of recesses (see Fig. 19) between gate contacts disposed in a first region of the semiconductor wafer; depositing a conductive material (6) (see Fig. 31) to fill the recesses and to cover the gate contacts such that a continuous conductive laver of the conductive material fills a first recess, extends over a gate contact and fills a second recess (see Fig. 32 and 33) (see Figs. 4-33);

However, Hamamoto does not disclose depositing a metal layer, wherein the metal layer contacts at least a portion of the continuous conductive layer and is in electrical contact with the continuous conductive layer filling the recesses.

Sung et al. disclose depositing of a metal layer (44) in direct contact with the conductive layer (40) filling the recesses in order to form that low resistant metal contact layer (see Fig. 10).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Hamamoto reference with depositing of a metal layer in direct contact with the conductive layer filling the recesses as taught by Sung et al. in order to form low resistant metal contact layer on the conductive layer (see Fig. 1A).

Re claim 2, as applied to claim 1 above, Hamamoto and Sung et al. in combination disclose all the claimed limitations including the limitation depositing an insulating layer over the conductive layer prior to depositing the metal layer; patterning a bitline mask on the

insulating layer; and etching selected portions of the insulating layer in accordance with the bitline mask to form a trench through the insulating layer to contact the conductive layer, wherein the metal layer is deposited in the trench (see Hamamoto Figs. 4-33 and Sung et al. Fig. 1A).

Re claim 3, as applied to claim 2 above, Hamamoto and Sung et al. in combination disclose all the claimed limitations including the limitation wherein etching the selected portions of the insulating layer is performed using a RIE process (see Hamamoto Figs. 4-33 and Sung et al. Fig. 1A).

Re claim 4, as applied to claim 3 above, Hamamoto and Sung et al. in combination disclose all the claimed limitations including the limitation wherein the RIE process includes over etching of through the insulating layer to ensure exposure of the conductive layer and the conductive covers top surfaces of the gate contacts after the RIE process (see Hamamoto Figs. 4-33 and Sung et al. Fig. 1A).

Re claim 5, as applied to claim 2 above, Hamamoto and Sung et al. in combination disclose all the claimed limitations including the limitation wherein the insulating layer comprises an oxide (see Hamamoto Figs. 4-33 and Sung et al. Fig. 1A).

Re claim 8, as applied to claim 1 above, Hamamoto and Sung et al. in combination disclose all the claimed limitations including the limitation wherein the metal layer comprises a refractory metal (see Hamamoto Figs. 4-33 and Sung et al. Fig. 1A).

Re claim 44, as applied to claim 38 in Paragraph 5, Hamamoto disclose all the claimed limitations.

However, Hamamoto does not disclose depositing a metal layer, wherein the metal layer contacts at least a portion of the continuous conductive layer and is in electrical contact with the continuous conductive layer filling the recesses.

Sung et al. disclose depositing of a metal layer (44) in direct contact with the conductive layer (40) filling the recesses in order to form that low resistant metal contact layer (see Fig. 10).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Hamamoto reference with depositing of a metal layer in direct contact with the conductive layer filling the recesses as taught by Sung et al. in order to form low resistant metal contact layer on the conductive layer (see Fig. 1A).

Re claim 45, as applied to claim 44 above, Hamamoto and Sung et al. in combination disclose all the claimed limitations including the limitation wherein the metal layer comprises a refractory metal (see Hamamoto Figs. 4-33 and Sung et al. Fig. 1A).

7. Claims 9 and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hamamoto (US/6,521,938) and Sung et al. (US/5,814,862), as applied to in Paragraph 6 above, and further in view of Nitayama et al. (US/6,236,079).

Re claims 9 and 46, as applied in clams 8 and 45 in Paragraph 6 above, Hamamoto and Sung et al. disclose all the claimed limitations including forming the refractory metal.

However, Hamamoto and Sung et al. do not disclose the refractory metal is being tungsten.

Nitayama et al. disclose method of forming a semiconductor device the method includes

depositing of tungsten metal (W) (102) (see Fig. 5I) to fill the recess in contact with the portion of conductive poly-Si layer (106). As shown in Fig. 5I, Nitayama et al. disclose that tungsten (W) (102) formed in conductively contact with the poly-Si layer in order to form the bit-line.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Hamamoto and Sung et al. reference with a refractory conductive metal comprises tungsten as taught by Nitayama et al. in order form the bit-line and connect the bit-line to the bit-line contact.

45. The method of claim 44 wherein the metal layer comprises tungsten.

8. Claims 10, 11, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hamamoto (US/6,521,938) and Sung et al. (US/5,814,862), as applied to in Paragraph 6 above, and further in view of Parekh et al. (US/6,383,868).

Re clams 10, 11, and 14, as applied to claim 1 in Paragraph 6 above, Hamamoto and Sung et al. disclose all the claimed limitations including forming of a conductive layer (plug).

However, Hamamoto and Sung et al. do not specifically disclose the conventional conductive material of silicon that comprises poly-silicon to form plug and doping the silicon plug.

Parekh et al. discloses forming doped polysilicon conductive layer (51) in the contact holes (50) in order to form self aligned contact plug (see Parekh et al. Fig. 1, Col. 4, lines 37-64).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Hamamoto and Sung et al. reference with doped silicon conductive material such as doped polysilicon as taught by Parekh et al. in order to form self aligned contact plug.

9. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over over Hamamoto (US/6,521,938), Sung et al. (US/5,814,862) and Parekh et al.,(US/6,383,868), as applied to claim 10 in Paragraph 8 above, and further in view of Taniguchi et al. (US/6,690,050).

Re claims 12 and 13, as applied to claim 10 in Paragraph 8 above, Hamamoto, Sung et al. and Parekh et al. in combination disclose all the claimed limitations including forming of a conductive layer (plug) comprising silicon (polysilicon).

However, Hamamoto, Sung et al. and Parekh et al. do not specifically disclose the conventional conductive material of silicon that comprises amorphous silicon and annealing of the amorphous silicon.

Taniguchi et al. disclose method of fabricating memory cell the method comprises forming of conductive silicon plug of amorphous silicon (31) and annealing of the amorphous silicon to convert the amorphous silicon to polysilicon (see Taniguchi et al. Fig. 7; Col. 6, line 48 – Col. 9, line 59; Col. 25, lines 44-52).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Hamamoto, Sung et al. and Parekh et al. reference with form an amorphous silicon and anneal the amorphous silicon as taught by Taniguchi et al. in order to form self aligned polysilicon contact plug.

10. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hamamoto (US/6,521,938) and Sung et al. (US/5,814,862), as applied in Paragraph 6 above, further in view of Wolf et al., (Silicon Processing for The VLSI Era, Volume 1: Process Technology, Pp. 184, (1986)).

Re claims 6 and 7, as applied in claim 5 in Paragraph 6 above, Hamamoto and Sung et al. disclose all the claimed limitations including forming of an oxide layer.

However, Hamamoto Sung et al. do not specifically disclose use of TOES precursor to form the oxide layer having a thickness least 1000 Å thick.

Wolf et al. disclose forming of silicon oxide by LPCVD process using TOES precursor. Wolf et al. disclose that TEOS films generally show excellent conformality (see Wolf et al. Page 184).

One of ordinary skill in the art would have been motivated to use TEOS precursor in order to form conformal silicon oxide film.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Hamamoto and Sung et al. reference with TEOS precursor to form an oxide layer as taught by Wolf et al. in order to form conformal silicon oxide film.

Furthermore, the claimed thickness would have been formed within the level of ordinary skill in the art by routine optimization in order to achieve the desired device size and performance.

Notwithstanding, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that

the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966). See *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955). Furthermore, the specification contains no disclosure of either the critical nature of the claimed thickness range or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919, f.2d 1575, 1578, 16 USPQ2d, 1936 (Fed. Cir. 1990).

Response to Arguments

11. Applicants' arguments with respect to claims 1-15 and 38-47 have been considered but are moot in view of the new ground(s) of rejection that was necessitated by the amendment filed on February 25, 2005.

Conclusion

12. **THIS ACTION IS MADE NON-FINAL.**

Correspondence

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (571) 272-1862. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brook Kebede
Examiner
Art Unit 2823

Brook Kebede

BK
March 21, 2005